Series Resonant Converter with Output Voltage Doubler

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Abstract—This paper presents a parallel zero voltage switching (ZVS) dc-dc converter with series connected transformers. In order to increase output power, two transformers connected in series are used in the proposed converter. Two buck-type converters connected in parallel have the same switching devices. The primary windings of series connected transformers can achieve the balanced secondary winding currents. The current doubler rectifiers with ripple current cancellation are connected in parallel at the output side to reduce the current stress of the secondary winding. Thus the current ripple on the output capacitor is reduced and the size of output choke and output capacitor are reduced. Only two switches are used in the proposed circuit instead of four switches in the conventional parallel ZVS converter to achieve zero voltage switching and output current sharing. Therefore, the proposed converter has less power switches. The ZVS turn-on is implemented during the commutation stage of two complementary switches such that the switching losses and thermal stresses on the semiconductors are reduced. Experimental results for a 528W (48V/11A) prototype are presented to prove the theoretical analysis and circuit performance.

Keywords—series connected transformers, parallel converters, converters.

I. INTRODUCTION

To reduce the environmental pollution and save energy waste, EPA (Environment Protection Agency) and CSCI (Climate Saver Computing Initiative) have been proposed the necessary circuit efficiency of modern power supply unit. For consumer power electronics, the small package size and high efficiency of power supply are also demanded. Two ways to achieve high efficiency power converters, there are the single-stage power converters for low power applications and two-stage power converters for medium and high power applications. Single-stage power converters are used in the applications of the electronic ballasts and light emitting diodes (LED) street lighting system. For two-stage power converters, the front-end stage with power factor correction (PFC) is usually adopted to reduce current harmonics and reactive power with 93–95% efficiency. Soft switching techniques have been proposed in [1]-[7] to achieve high efficiency dc-dc converter. However, the main drawback of these techniques is high voltage or current stresses on power semiconductors to limit the practical applications in power supply unit. In series resonant converter, the output voltage cannot be properly regulated at no-load condition. The LLC series resonant converter has been drawn attention due to its essential advantages of high conversion efficiency and high power density [8]-[14]. The half-bridge or full-bridge converter type is usually adopted at the primary side to realize the zero voltage switching (ZVS) turn-on for all power switches without any auxiliary circuit. If the switching frequency is lower than the series resonant frequency, the secondary side rectifier is operated under zero current switching (ZCS) condition. Then the reverse recovery losses for diode rectifier or the switching losses for synchronous rectifier are reduced.

This paper presents a parallel LLC series resonant converter for server/data storage system applications. In the proposed converter, two converter cells are connected in parallel to share the input and load current. The output voltage doubler is adopted in the secondary side to reduce the secondary winding turns and to clamp the voltage stress of the rectifier diodes to output voltage. Thus the low voltage rating schottky diodes can be used in the secondary side. The design switching frequency at full load condition is less than series resonant frequency. Thus the power switches in the primary side are operated at ZVS turn-on and the rectifier diodes in the secondary side are operated at ZCS turn-off. Therefore, the switching losses of power switches and reverse recovery losses of rectifier diodes are reduced. The fundamental frequency approximation technique is adopted to derive the voltage conversion ratio and the circuit parameters. A design procedure of the proposed converter is presented in detail. Experiments based on a 960W prototype for server power supply unit were provided to verify the effectiveness of the proposed converter.

II. CIRCUIT CONFIGURATION

The circuit configuration of the proposed converter is shown in Fig. 1. Compared with other soft switching converters such as asymmetry half-bridge converters and active clamp converters, the adopted LLC converter can achieve ZVS turn-on of power switches with the wide range of load conditions and input voltage range. The rectifier diodes can be turned off at ZCS if the switching frequency is less than the series resonant frequency. Thus the switching losses are reduced. The output terminal voltage is controlled by variation of switching frequency. Two LLC circuits with output voltage doubler are connected in parallel to share the load current. Thus the current stresses at the secondary windings are reduced. $V_o$ and $V_{o1}$ are input and output terminal voltages, respectively. In circuit 1, switches $Q_1$ and $Q_2$ are...
half-bridge network, \( C_{\text{r1}}, L_{\text{r1}}, \) and \( L_{\text{m}} \) are resonant tank, \( T_j \) is an isolated transformer, and \( D_1 \) and \( D_2 \) are rectifier diodes. \( C_{\text{oss1}} \) and \( C_{\text{oss2}} \) are output capacitances of switches \( Q_j \) and \( Q_k \) respectively. In the same manner, the circuit 2 includes the circuit components of \( Q_3, Q_4, C_{\text{r2}}, L_{\text{r2}}, L_{\text{m}} \), \( T_2 \), \( D_3 \) and \( D_4 \). The output voltage doubler rectifier is adopted to reduce the secondary winding turns compared with the center-tapped rectifier topology. The voltage stress of rectifier diodes is clamped to output terminal voltage \( V_o \). There is only a diode voltage drop at the secondary side instead of two diode voltage drop in the full-wave diode rectifier. The proposed voltage drop at the secondary side instead of two diode module, server power supply unit and data storage power PC power supply, LCD-TV power module, PDP-TV power used in medium power rating applications such as all-in-one computer, and on/off states of switches and rectifier diodes, there are eight operation modes in a switching cycle. Fig. 2 and Fig. 3 give the main key waveforms and the topological equivalent circuits in a switching cycle. Before time \( t_0 \), \( Q_j \) and \( Q_k \) are on and the resonant inductor current \( i_{L_j}=i_{L_{m1}} \) and \( i_{L_k}=i_{L_{m2}} \). All rectifier diodes \( D_1 \sim D_4 \) are off. Mode 1 \( [t_0 \leq t_1] \): At time \( t_0 \), switches \( Q_j \) and \( Q_k \) are turned off and diodes \( D_1 \) and \( D_2 \) are conducting in this mode. The magnetizing inductance voltages \( v_{L_{m1}} \) and \( v_{L_{m2}} \) are clamped to \( nV_{o1} \) and \( -nV_{o2} \) respectively. The magnetizing current \( i_{L_{m1}} \) increases and \( i_{L_{m2}} \) decreases in this mode.

\[
\begin{align*}
   i_{L_{m1}}(t) &= i_{L_{m1}}(t_0) + nV_{o1} (t-t_0) / L_m, \\
   i_{L_{m2}}(t) &= i_{L_{m2}}(t_0) - nV_{o2} (t-t_0) / L_m.
\end{align*}
\]

(1)

where \( n=N_j/N_k \) and \( L_{m1}=L_{m2}=L_m \), \( C_{\text{oss1}}, C_{\text{oss2}}, C_{\text{r1}} \) and \( L_{r1} \) are resonant in circuit 1 and \( C_{\text{oss3}}, C_{\text{oss4}}, C_{\text{r2}} \) and \( L_{r2} \) are resonant in circuit 2. The inductor current \( i_{L_{r1}} \) charges capacitor \( C_{\text{oss2}} \) from zero voltage and discharges capacitor \( C_{\text{oss1}} \) from \( V_{in} \). In the same manner, Capacitor \( C_{\text{oss3}} \) is charged from zero voltage and capacitor \( C_{\text{oss4}} \) is discharged from \( V_{in} \). The capacitor voltages are approximately expressed as:

\[
\begin{align*}
   v_{C_{\text{oss1}}}(t) &= V_{in} - \frac{i_{L_{r1}}(t_0)}{2C_{\text{oss}}} (t-t_0), \\
   v_{C_{\text{oss2}}}(t) &= \frac{i_{L_{r1}}(t_0)}{2C_{\text{oss}}} (t-t_0), \\
   v_{C_{\text{oss3}}}(t) &= \frac{i_{L_{r2}}(t_0)}{2C_{\text{oss}}} (t-t_0), \\
   v_{C_{\text{oss4}}}(t) &= v_{C_{\text{oss3}}}(t) \approx V_{in} - \frac{i_{L_{r2}}(t_0)}{2C_{\text{oss}}} (t-t_0) \quad (2)
\end{align*}
\]

The secondary winding currents \( i_{Q1} \) and \( i_{Q2} \) are given as:

\[
\begin{align*}
   i_{Q1}(t) &= n[i_{L_{r1}}(t)-i_{L_{m1}}(t)], \\
   i_{Q2}(t) &= n[-i_{L_{r2}}(t)+i_{L_{m2}}(t)]. \quad (3)
\end{align*}
\]

At time \( t_1 \), the voltages \( v_{C_{\text{oss2}}} \) and \( v_{C_{\text{oss3}}} \) equal \( V_{in} \) and \( v_{C_{\text{oss1}}} \) and \( v_{C_{\text{oss4}}} \) equal 0. Then the anti-parallel diode of \( Q_j \) and \( Q_k \) is conducting.

Mode 2 \( [t_1 \leq t_2] \): At time \( t_1 \), the anti-parallel diodes of \( Q_1 \) and \( Q_4 \) are conducting. In the secondary side, the rectifier diodes \( D_1 \) and \( D_4 \) are forward-biased to charge capacitor voltage \( V_{o1} \) and \( V_{o2} \) respectively. Since the switch currents \( i_{Q2} \) and \( i_{Q4} \) are negative in this mode, switches \( Q_j \) and \( Q_k \) can be turned on in this interval to realize ZVS. This mode ends at time \( t_2 \) when \( Q_j \) and \( Q_k \) are turned on.

Mode 3 \( [t_2 \leq t_3] \): At time \( t_2 \), \( Q_j \) and \( Q_k \) are turned on at ZVS (since \( i_{Q2}(t_2)=0 \) and \( i_{Q4}(t_2)=0 \)). The rectifier diodes \( D_1 \) and \( D_4 \) are conducting in this mode. Thus the magnetizing inductor voltages \( v_{L_{m1}}=-nV_{o1} \) and \( v_{L_{m2}}=-nV_{o2} \). The magnetizing current \( i_{L_{m1}} \) increases linearly with the slope of \( nV_{o1}/L_m \) and the magnetizing current \( i_{L_{m2}} \) decreases linearly with the slope of \( -nV_{o2}/L_m \). \( C_{\text{r1}} \) and \( C_{\text{r2}} \) are resonant with the applied voltage \( V_{in} \) and \( V_{in} \) in circuit 1 and \( L_{r1} \) and \( C_{\text{r2}} \) are resonant with the applied voltage \( -nV_{o2} \) in circuit 2. The resonant frequency of circuits 1 and 2 in this mode is derived as:

\[
   f_r = \frac{1}{2\pi \sqrt{L_r C_r}} \quad (3)
\]
The resonant inductor currents and capacitor voltages during this interval are expressed as:

\[
i_{Lr1}(t) = \frac{V_{in} - nV_{o1} - v_{C1}(t)}{L_r/C_r} \sin \frac{t-t_2}{L_r/C_r} + i_{Lr1}(t_2) \cos \frac{t-t_2}{L_r/C_r} \tag{4}
\]

\[
i_{Lr2}(t) = \frac{nV_{o2} - v_{C2}(t)}{L_r/C_r} \sin \frac{t-t_2}{L_r/C_r} + i_{Lr2}(t_2) \cos \frac{t-t_2}{L_r/C_r} \tag{5}
\]

\[
v_{C1}(t) = V_{in} - nV_{o1} - [V_{in} - nV_{o1} - v_{C1}(t_2)] \cos \frac{t-t_2}{L_r/C_r} + i_{Lr1}(t_2) \frac{L_r}{C_r} \sin \frac{t-t_2}{L_r/C_r} \tag{6}
\]

\[
v_{C2}(t) = nV_{o2} - [nV_{o2} - v_{C2}(t_2)] \cos \frac{t-t_2}{L_r/C_r} + i_{Lr2}(t_2) \frac{L_r}{C_r} \sin \frac{t-t_2}{L_r/C_r} \tag{7}
\]

The resonant inductor current \(i_{Lr1}\) increases and \(i_{Lr2}\) decreases. In circuit 1, the power is transferred from input terminal voltage \(V_{in}\) to output voltage \(V_{o1}\) through \(C_{r1}, L_{r1}, T_1\) and \(D_1\). In circuit 2, the energy stored in resonant inductance \(L_{r2}\) is transferred to output voltage \(V_{o2}\) through \(C_{r2}, L_{r2}, T_2\) and \(D_4\). This mode ends at time \(t_3\) when \(i_{Lm1}=i_{Lr1}\) and \(i_{Lm2}=i_{Lr2}\). Then the diode currents \(i_{D3}=i_{D4}=0\) and diodes \(D_1\) and \(D_4\) go to turn off.
Mode 4 \([t_5 \leq t < t_6]\): This mode starts at \(t_5\) when \(i_{Lm1} = i_{Lr1}\) and \(i_{Lm2} = i_{Lr2}\). Then all the secondary diodes \(D_1 - D_4\) are off. However, switches \(Q_1\) and \(Q_2\) are still on. Thus the components \(C_{r1}\), \(L_{r1}\) and \(L_{m1}\) in circuit 1 are resonant. In the same manner, \(C_{r2}\), \(L_{r2}\) and \(L_{m2}\) in circuit 2 are resonant in this interval. The resonant frequency is given as:

\[
f_p = \frac{1}{2\pi\sqrt{L_m + L_r}}C_r
\]  

(8)

The resonant inductor currents and capacitor voltages during this interval are expressed as:

\[
i_{Lr1}(t) = -\frac{V_{in} - v_{C_{r1}}(t_3)}{\sqrt{(L_r + L_m)}/C_r} \sin \frac{t - t_3}{\sqrt{(L_r + L_m)}C_r} + i_{Lr1}(t_3) \cos \frac{t - t_3}{\sqrt{(L_r + L_m)}C_r}
\]

(9)

\[
i_{Lr2}(t) = -\frac{v_{C_{r2}}(t_3)}{\sqrt{(L_r + L_m)}/C_r} \sin \frac{t - t_3}{\sqrt{(L_r + L_m)}C_r} + i_{Lr2}(t_3) \cos \frac{t - t_3}{\sqrt{(L_r + L_m)}C_r}
\]

(10)

\[
v_{C_{r1}}(t) = V_{in} - \frac{v_{C_{r1}}(t_3)}{\sqrt{(L_r + L_m)}/C_r} \sin \frac{t - t_3}{\sqrt{(L_r + L_m)}C_r} + i_{Lr1}(t_3) \cos \frac{t - t_3}{\sqrt{(L_r + L_m)}C_r}
\]

(11)

\[
v_{C_{r2}}(t) = v_{C_{r2}}(t_3) \cos \frac{t - t_3}{\sqrt{(L_r + L_m)}C_r} + i_{Lr2}(t_3) \cos \frac{t - t_3}{\sqrt{(L_r + L_m)}C_r}
\]

(12)

In this mode, the resonant inductor current \(i_{Lr1} = i_{Lm1}\) and \(i_{Lr2} = i_{Lm2}\). This mode ends at time \(t_6\) when switches \(Q_1\) and \(Q_2\) are turned off.

Mode 5 \([t_5 \leq t < t_6]\): At time \(t_5\), \(Q_1\) and \(Q_2\) are turned off and diodes \(D_2\) and \(D_4\) are conducting. The magnetizing inductance voltages \(v_{Lm1}\) and \(v_{Lm2}\) are clamped to \(-nV_{o2}\) and \(nV_{o1}\), respectively. The magnetizing current \(i_{Lm}\) decreases with the slope of \(-nV_{o2}/L_m\) and \(i_{Lm2}\) increases with the slope of \(nV_{o1}/L_m\) in this mode. At time \(t_6\), the inductor currents \(i_{Lr1}\) and \(i_{Lr2}\) are positive and negative, respectively. \(C_{oss1}\) and \(C_{oss2}\) are charged and discharged respectively by inductor current \(i_{Lr}\). In the same manner, \(C_{oss3}\) and \(C_{oss4}\) are charged and discharged respectively by inductor current \(i_{Lr}\). If the energy stored in the inductor \(L_{r1}\) is greater than the energy stored in capacitors \(C_{oss1}\) and \(C_{oss2}\), then capacitor \(C_{oss}\) can be charged to \(V_{in}\) and \(C_{oss2}\) can be discharged to zero voltage. The drain to source voltages of \(Q_3\) and \(Q_4\) are derived as:

\[
v_{Q3,ds}(t) = v_{C_{oss1}}(t) \approx \frac{i_{Lr1}(t_4)}{2C_{oss}}(t - t_4)
\]

\[
v_{Q4,ds}(t) = v_{C_{oss2}}(t) \approx V_{in} - \frac{i_{Lr1}(t_4)}{2C_{oss}}(t - t_4)
\]

(13)

Likewise, the drain to source voltages of \(Q_3\) and \(Q_4\) are derived as:

\[
v_{Q3,ds}(t) = v_{C_{oss1}}(t) \approx \frac{i_{Lr2}(t_4)}{2C_{oss}}(t - t_4)
\]

\[
v_{Q4,ds}(t) = v_{C_{oss2}}(t) \approx V_{in} - \frac{i_{Lr2}(t_4)}{2C_{oss}}(t - t_4)
\]

(14)

The secondary winding currents \(i_{D2}\) and \(i_{D3}\) are given as:

\[
i_{D2}(t) = n(-i_{Lr1}(t) + i_{Lm1}(t_1)) = n(-i_{Lr2}(t) - i_{Lm2}(t_2)(t))
\]

At time \(t_5\), the capacitor voltages \(v_{C_{oss1}}\) and \(v_{C_{oss2}}\) equal zero voltage. Then the anti-parallel diode of \(Q_2\) and \(Q_3\) is conducting.

Mode 6 \([t_6 \leq t < t_7]\): At time \(t_6\), the anti-parallel diode of \(Q_2\) and \(Q_3\) is conducting \((i_{Lr1}(t_5) > 0\) and \(i_{Lr2}(t_5) < 0\). The secondary diodes \(D_2\) and \(D_4\) are conducting in this mode. Thus the magnetizing inductor voltages \(v_{Lm1} = -nV_{o2}\) and \(v_{Lm2} = nV_{o1}\). The magnetizing currents \(i_{Lm1}\) and \(i_{Lm2}\) decrease and increases respectively. Since the switch currents \(i_{D2}\) and \(i_{D3}\) are both negative in this mode, switches \(Q_2\) and \(Q_3\) can be turned on in this interval to realize ZVS. This mode ends at time \(t_7\) when \(Q_2\) and \(Q_3\) are turned on.

Mode 7 \([t_6 \leq t < t_7]\): At time \(t_6\), \(Q_3\) and \(Q_4\) are both turned on at ZVS (since \(i_{D2}(t_5) > 0\) and \(i_{D4}(t_5) < 0\)). The rectifier diodes \(D_2\) and \(D_4\) are conducting in this interval and the magnetizing inductor voltages \(v_{Lm1} = -nV_{o2}\) and \(v_{Lm2} = nV_{o1}\). The magnetizing current \(i_{Lm1}\) decreases linearly with the slope of \(-nV_{o2}/L_m\). Likewise, the inductor current \(i_{Lm2}\) increases linearly with the slope of \(nV_{o1}/L_m\). \(L_{r1}\) and \(C_{r1}\) are resonant with the applied voltage \(-nV_{o2}\) in circuit 1 and \(L_{r2}\) and \(C_{r2}\) are resonant with the applied voltage \(nV_{o1}\) in circuit 2. The resonant inductor currents and capacitor voltages during this interval are expressed as:

\[
i_{Lr1}(t) = \frac{nV_{o2} - v_{C_{r1}}(t_6)}{L_r/C_r} \sin \frac{t - t_6}{L_r/C_r} + i_{Lr1}(t_6) \cos \frac{t - t_6}{L_r/C_r}
\]

(16)

\[
i_{Lr2}(t) = \frac{V_{in} - nV_{o1} - v_{C_{r2}}(t_6)}{L_r/C_r} \sin \frac{t - t_6}{L_r/C_r} + i_{Lr2}(t_6) \cos \frac{t - t_6}{L_r/C_r}
\]

(17)

\[
v_{C_{r1}}(t) = nV_{o2} - \frac{nV_{o2} - v_{C_{r1}}(t_6)}{L_r/C_r} \sin \frac{t - t_6}{L_r/C_r} + i_{Lr1}(t_6) \cos \frac{t - t_6}{L_r/C_r}
\]

(18)

\[
v_{C_{r2}}(t) = \frac{V_{in} - nV_{o1} - v_{C_{r2}}(t_6)}{L_r/C_r} \sin \frac{t - t_6}{L_r/C_r} + i_{Lr2}(t_6) \cos \frac{t - t_6}{L_r/C_r}
\]

(19)

The resonant inductor current \(i_{Lr1}\) decreases and \(i_{Lr2}\) increases. In circuit 1, the energy stored in resonant inductance \(L_{r1}\) is transferred to output voltage \(V_{o2}\) through \(C_{r1}, L_{r1}, T_1\) and \(D_2\). In circuit 2, the power is transferred from input terminal voltage \(V_{in}\) to output voltage \(V_{o1}\) through \(C_{r2}, L_{r2}, T_2\) and \(D_3\). This mode ends at time \(t_7\) when \(i_{Lm1} = i_{Lr1}\) and \(i_{Lm2} = i_{Lr2}\). Then diode currents \(i_{D2} = i_{D3} = 0\) and all diodes \(D_1 - D_4\) are off.

Mode 8 \([t_7 \leq t < t_8]\): This mode starts at \(t_7\) when \(i_{Lm1} = i_{Lr1}\) and \(i_{Lm2} = i_{Lr2}\). Thus all rectifier diodes \(D_1 - D_4\) are off. Since \(Q_2\) and \(Q_3\) are still conducting, the components \(C_{r1}, L_{r1}\) and \(L_{m1}\) in
circuit 1 are resonant. Likewise, $C_{r2}$, $L_{r2}$ and $L_{m2}$ in circuit 2 are resonant in this interval. The resonant inductor currents and capacitor voltages during this interval are expressed as:

$$i_{Lr1}(t) = -\frac{V_{C1}(t)}{(L_r + L_m)/C_r} \sin \frac{t_{r1} - t}{(L_r + L_m)C_r}$$

$$+ i_{Lr2}(t) \cos \frac{t - t_{r1}}{(L_r + L_m)C_r}$$

$$v_{C1}(t) = v_{C1}(t) \cos \frac{t - t_{r1}}{(L_r + L_m)C_r}$$

$$v_{C2}(t) = v_{in} - v_{C2}(t) \cos \frac{t - t_{r1}}{(L_r + L_m)C_r}$$

$$+ i_{Lr2}(t) \sqrt{\frac{L_r + L_m}{C_r}} \sin \frac{t - t_{r1}}{(L_r + L_m)C_r}$$

In this mode, the resonant inductor current $i_{Lr1} = i_{Lm1}$ and $i_{Lr2} = i_{Lm2}$. This mode ends at time $t_0$ when switches $Q_2$ and $Q_3$ are turned off. Then one switching cycle is completed.

### IV. SYSTEM ANALYSIS AND DESIGN EXAMPLE

#### A. System Analysis

The output voltage of the adopted converter is controlled with the pulse frequency modulation with 50% duty cycle for each power switch. The fundamental harmonic analysis is used to derive the dc voltage conversion ratio. The power transfer from input terminal to output load through the resonant tank is associated to the fundamental switching frequency. Thus the harmonics of the switching frequency are neglected in the following system analysis. Fig. 4(a) shows the equivalent circuit for each converter module. Since the duty cycle of switches $Q_1$ and $Q_2$ is 0.5, the input voltage to the resonant tank $v_{Q2,ds}$ is a square waveform between 0 and $V_{in}$. Based on the Fourier series analysis, the input voltage $v_{Q2,ds}$ can be given as:

$$v_{Q2,ds} = \frac{V_{in}}{2} + \sum_{m=1,3,5,...}^\infty \frac{2V_{in}}{\pi m} \sin(2\pi mf_s t)$$

The root-mean-square (rms) value of the fundamental input voltage and input current can be expressed as:

$$V_{Q2,f} = \sqrt{2}V_{in}/\pi, \quad I_{Lr1,f} = \sqrt{2}I_{Lr1,1} \sin(2\pi f_s t - \theta)$$

where $I_{Lr1,f}$ and $\theta$ are the rms value and phase shift of fundamental input current $i_{Lr1}$. The output side of the proposed converter is driven by a quasi-sinusoidal current. If the inductor current $i_{Lr1} = i_{Lm1}$, the rectifier diode $D_{1}$ is conducting and $v_{Lm} = nV_{o}$. If $i_{Lr1} < i_{Lm1}$, then $v_{Lm} = nV_{o}$. We assumed that the time intervals in modes 1, 2, 5 and 6 can be neglected, the transformer primary voltage is a quasi-square waveform and can be expressed as:

$$v_{Lm1} = \sum_{m=1,3,5,...}^\infty \frac{2nV_o}{\pi m} \sin(2\pi mf_s t - \theta_m)$$

where $\theta_m$ is the phase angle of $m$-th harmonic frequency. The rms value of the fundamental primary voltage is derived as $v_{Lm1,f} = \sqrt{2}nV_o/\pi$. Thus, the load resistance reflected to the transformer primary side is give as:

$$R_{ac} = \frac{v_{Lm1,f}}{i_{Lr1,f}} = \frac{4n^2}{\pi^2}R_o$$

Therefore the ac resonant tank is excited by an effectively sinusoidal input voltage $V_{Q2,f}$ and drives an effective resistive road $R_{ac}$. Fig. 4(b) shows the ac equivalent circuit. The input impedance of the resonant tank is given as:

$$Z_{in}(s) = \frac{V_{Q2,f}(s)}{I_{Lr1,1}(s)} = \frac{1}{sC_r} + sL_r + \frac{sL_m R_{ac}}{sL_m + R_{ac}}$$

The ac voltage gain related to the switching frequency is derived as:

$$|G_{ac}(f)| = \frac{sL_m R_{ac}}{Z_{in}(s)} = \sqrt{\frac{1}{1+k(1-f_s^2)}} + Q^2(f_s - f_r)^2$$

where $k = L_r/L_m$, $Q = \sqrt{L_r/C_r}$ and $f_r = 1/2\pi\sqrt{L_rC_r}$.

Under no-load condition ($R_{ac}=\infty$), $Q=0$ and $f_r=\infty$, the minimum ac voltage gain at no-load condition is derived as:

$$|G_{ac}(f)|_{NL,f_r=\infty} = \frac{1}{1+k}$$

Thus the proposed converter can be controlled at no load condition if the design minimum voltage gain at maximum input voltage meets the following condition.
\[ G_{dc,\text{min}} = \frac{2n(V_0/2+V_f)}{V_{in,max}} > \frac{1}{(1+k)} \]  

where \( V_f \) is the voltage drop on rectifier diodes \( D_1\sim D_4 \).

V. EXPERIMENTAL RESULTS

Experimental results based on a 960W laboratory prototype for server power supply unit were presented to verify the effectiveness of the proposed converter. The circuit parameters of the laboratory prototype with 960W rated power are derived in this section and shown in Fig. 5. The front stage of the proposed converter is a PFC boost converter to supply the stable 390V input terminal voltage. Fig. 6 shows the measured gate voltages of four power switches in the proposed converter. Fig. 7 shows the gate voltages and drain voltages of \( Q_1\sim Q_4 \) at full load condition \( (P_o=960W) \). It is clear that the drain voltage has been decreased to zero before the gate voltage is high. Thus the ZVS turn-on of switches is realized and the switching losses on power switches can be reduced. Fig. 8 shows the gate voltage, drain voltage and switch current of switch \( Q_1 \) at 100% of full load conditions. Fig. 9 shows the measured waveforms \( v_{Q1,gs}, v_{Cr1}, i_{Lr1}, v_{O2} \) and \( i_{Lr2} \) at 100% of full load conditions.

Fig. 10 illustrates the measured waveforms of gate voltage \( v_{Q1,gs} \) and diode currents \( i_{D1}\sim i_{D4} \) at 100% of full loads. The measured gate voltage \( v_{Q1,gs} \) and output capacitor voltages \( V_{o1} \) and \( V_{o2} \) at 100% of full load are shown in Fig. 11. Fig. 12 illustrates the measured results of \( v_{Q1,gs}, i_{D1}+i_{D3}, i_{D2}+i_{D4} \) and \( i_o \) at full load. We can observe that two resultant currents \( i_{D1}+i_{D3}, \) \( i_{D2}+i_{D4} \) before output capacitors are balanced.
VI. CONCLUSION

This paper presents a parallel LLC converter to share the load current and reduce the ripple current on the input side. Based on the designed high voltage gain, the switching frequency is less than the series resonant frequency at full load. Thus the power switches are turned on at ZVS and rectifier diodes are turned off at ZCS. The switching loss on power switches is reduced and reverse recovery current on rectifier diodes is eliminated. The output voltage doubler topology is used in the secondary side to reduce the secondary winding in the conventional center-tapped rectifier and the voltage stress of output diode is clamped to output terminal voltage instead of two times of output voltage in the conventional center-tapped rectifier. The fundamental harmonic analysis method is adopted to derive the voltage conversion ratio. The proposed converter can also regulate output voltage at no-load condition with the properly voltage gain design. The design procedure and design example are provided to obtain the component parameters of the proposed converter. Finally experiments based on a 960W prototype are provided to verify the effectiveness of the converter.

REFERENCES